REMARKS

Claims 1-20 are all the claims presently pending in the application. Claims 3 and 13 have been amended to more particularly define the invention. New claims 15-20 have been added to claim additional features of the invention and to provide more varied protection for the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability.

Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 3 and 13 stand rejected upon informalities (e.g., 35 U.S.C. § 112, second paragraph), and claims 1-14 stand rejected on prior art grounds. With respect to the prior art rejection, claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the applicant's admitted prior art (hereinafter "APA") in view of Kellogg, et al. (U.S. Patent No. 6,070,262; hereinafter "Kellogg").

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor memory device having an error check and correction (ECC) type error recovery circuit.

An illustrative, non-limiting embodiment of the semiconductor memory device, as defined by independent claim 1, includes a memory cell array including at least one normal memory cell array portion and an ECC memory cell array portion. The normal memory cell array portion includes a plurality of normal memory cells, and the ECC memory cell array portion includes a plurality of ECC memory cells. The device also includes an X decoder for selecting one of word lines in the memory cell array, wherein the word lines extend from the X decoder to the memory cell array, and an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line, the cell data including data from normal

cells and ECC cells of the selected word line, wherein the ECC memory cell array portion is disposed at a location other than the far end of the word lines from said X decoder.

In another exemplary embodiment, as defined by independent claim 11, the semiconductor memory device having an error check and correction (ECC) type error recovery circuit includes a memory cell array including a plurality of normal memory cell array portions and an ECC memory cell array portion. Each of the normal memory cell array portions includes a plurality of normal memory cells, and the ECC memory cell array portion includes a plurality of ECC memory cells. The device also includes an X decoder for selecting at least one of the word lines in the memory cell array, the word lines in the memory cell array, and the word lines extending from the X decoder to the memory cell array. The device also includes a Y decoder and digit lines extending from the Y decoder toward the memory cell array, and an ECC operation circuit for performing error check and correction based on cell data read out from a selected word line. The cell data includes data from normal cells and ECC cells of the selected word line, wherein the ECC memory cell array portion is disposed at a location other than the far end of the word lines from the X decoder.

In the present invention, the ECC cell array portion is disposed at a location in which read out speed of data from ECC cell or cells does not become the worst (e.g., slowest) speed in a memory device. That is, the ECC cell array portion is disposed at a location other than at the far end portion of the word lines, with respect to the X decoder. Thus, the normal cell array portion is disposed at a location in which the read out speed of data from a normal cell becomes the worst speed in a memory device. Accordingly, the worst read out speed of data can be measured from outside (e.g., the exterior), in order to perform a production test of memory devices, to analyze the cause of a defect in operation speed and the like.

Conventional memory devices that use the ECC type error recovery circuit have several disadvantages. For example, the ECC cells are disposed at far ends of the word lines from an X decoder, and thus, it is impossible to correctly measure, from outside the circuit, the slowest value of the reading out speed of the cell data. Additionally, in conventional memory cell devices, the ECC cells are disposed at the outermost portions of a memory cell array so that the

ECC cells can be omitted from the memory cell array in a memory device which does not need the cells (e.g., a memory cell device having a small memory capacity which would undesirably take up a large amount of area if it included the ECC cells). However, the rising (or falling) time of a word select signal becomes slow at the far end portion of a word line when compared with that at the near end portion on the side of an X address decoder, and therefore, a read out speed of cell data is slower at the far end portion of a word line.

In the claimed invention, as mentioned above, the ECC cell array portion is disposed at a location other than at the far end portion of the word lines, with respect to the X decoder. Thus, the normal cell array portion is disposed at a location in which the read out speed of data from a normal cell or cells becomes the worst speed in a memory device. Accordingly, the worst read out speed of data can be measured from outside, for example, to perform production tests of the memory devices, to analyze the cause of a defect in the operation speed, or the like.

Moreover, by disposing the ECC cell array portion substantially in the central portion of the memory cell array, the manufacturing yield of the semiconductor memory device can be improved because of an improvement in an error recovery rate. That is, the probability of a defect in a memory cell in the middle or central portion of the memory cell array is lower than the probability of a defect in a memory cell in the peripheral portion of the memory cell array.

II. THE 35 U.S.C. §112, SECOND PARAGRAPH REJECTION

Claims 3 and 13 stand rejected under 35 U.S.C. §112, second paragraph. The claims have been amended, above, to overcome this rejection. Specifically, claims 3 and 13 are amended merely to replace "approximately" with the term "substantially" in accordance with U.S. patent practice.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. CLAIM REJECTIONS BASED ON PRIOR ART GROUNDS

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the

Applicant's Admitted Prior Art (APA; particularly Figure 3) in view of Kellogg. For at least the following reasons, Applicant traverses this rejection.

The APA discloses a schematic structure of a conventional memory device having an ECC type error recovery circuit, and specifically an ECC cell array portion P1 which is disposed at the far end portion from the X decoder 3, such that the ECC cells can be easily omitted from the memory cell array in a memory device which does not need the ECC cells.

In the Office Action, the Examiner acknowledges that the APA in Figure 3 of the present invention discloses a conventional semiconductor device having an ECC type error recovery circuit, in which the ECC cell (i.e., portion P1) is disposed at the far end portion with respect to the X decoder, but that the APA does not explicitly teach that the ECC memory cell portion is disposed at a location other than the far end of the word line with respect to the X decoder. However, the Examiner takes the position that Kellogg makes up for the deficiencies of the APA.

Particularly, the Examiner asserts that Kellogg discloses an ECC array arranged at the near end of a decoder, as allegedly shown by element 164'. As such, the Examiner alleges that it would have been obvious to arrange the ECC memory locations of the APA in different areas (locations) of the memory device based on Kellogg for the purpose of heightening the decoding efficiency and increasing the flexibility of the configuration. Applicant respectfully disagrees for several reasons.

As the Examiner well knows, the mere fact that references may be capable of being combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of such a combination (see M.P.E.P. § 2143.01). The Examiner must present a convincing line of reasoning as to why the ordinary skilled artisan would have found the claimed invention to have been obvious in light of the teachings of the references, without the benefit of Applicant's own invention. In doing so, each reference as a whole must be considered for what it fairly teaches to a person of ordinary skill in the art.

In this case, the Office Action states that the motivation for modifying the APA based on Kellogg would be "*because disposing an ECC memory cell in different locations would heighten the decoding efficiency and increasing the flexibility of configuration.*"

However, it is respectfully noted that neither Kellogg nor the APA mentions either the "decoding efficiency" or "increasing the flexibility of configuration." Instead, Kellogg specifically mentions that the object of Kellogg is to improve reliability of high performance memory systems with error checking capability, not to improve memory speed (see col. 1, lines 43-50). Thus, the stated motivation is not supported by the applied references.

Absent a reasonable motivation or suggestion in the prior art references, or in the art in general, it would appear that the Office Action is using improper hindsight based analysis (i.e., using that which the inventor has taught against him). Thus, it is respectfully submitted that the Office Action fails to provide a convincing line of reasoning as to any reasonable suggestion or motivation for doing that which the inventor has done. Accordingly, a *prima facie* case of obviousness has not been established.

Irrespective of the Office Action's stated motivation, Applicant submits that a person of ordinary skill in the art would not have been motivated to modify the APA based on the teachings of Kellogg to arrive at the claimed invention. That is, Kellogg provides no suggestion or motivation for affirmatively and purposefully disposing the ECC memory cell array portion at a location other than the far end of the word lines from the X decoder, as claimed in claim 1.

For example, with reference to Figure 3, Kellogg specifically states that "in this example, sub-page array 164' is predesignated as the check bit array, although any sub-page may be chosen for the ECC array." (See col. 4, lines 6-8). That is, contrary to the claimed invention, Kellogg discloses that any location for the ECC array is acceptable, which presumably would include disposing the ECC array at the far end portion, similar to the APA.

Furthermore, Kellogg does not disclose, suggest, or even seem to recognize any advantages (or disadvantages) stemming from the location of the sub-page array 164' (i.e., the array designated as the check bit array). That is, Kellogg does not contemplate the problems that are addressed and solved by the claimed invention, or for that matter, recognize any advantages or disadvantages derived from disposing the ECC memory cell array portion at a location other than the far end. Thus, Applicant submits that Kellogg neither discloses nor suggests the desirability of modifying the APA to arrive at the claimed invention.

Assuming *arguendo* that it would have been obvious to combine the APA and Kellogg, Applicant submits that the resulting combination still would not arrive at the claimed invention.

For example, in Kellogg, the disposition (locational relationship) of an ECC memory cell array and a decoder is not shown clearly. Moreover, the function of the logic decoder described in Kellogg is different from that of an X decoder (word decoder) of the present invention.

Thus, Applicant submits that any combination of the APA and Kellogg would not arrive at the claimed invention, in as complete detail as recited in the claimed invention.

For at least the foregoing reasons, Applicant respectfully submits that the claimed invention would not have been obvious over the APA in view of Kellogg for any reason, since neither the APA, Kellogg, nor the art in general, provides any motivation or suggestion for doing that which the inventor has done. Accordingly, the § 103 rejection of claims 1-14 should be withdrawn.

Additionally, with respect to claims 2, 3, 12, and 13, the Office Action states that "*configuring the ECC cell array in different memory locations is common practice for most error recovery systems*", and therefore, that it would have been obvious to implement the ECC cell array in different memory locations in order to heighten the decoding efficiency and increase the flexibility of the configuration.

However, as the Examiner well knows, mere conclusory statements are not sufficient to establish a *prima facie* case of obviousness. It is noted that official notice, which is unsupported by documentary evidence, should only be taken where the facts asserted to be well-known, or to be common knowledge in the art, are capable of instant and unquestionable demonstration as being well-known. (See M.P.E.P. § 2144.03.) Applicant submits that configuring the ECC cell array in the novel manner claimed by Applicant is not common practice. However, if the Examiner maintains this position, the Examiner is respectfully requested in the next Office Action to cite a reference in support of this position.

For at least the foregoing reasons, Applicant submits that claims 1-14 would not have been obvious over the APA and Kellogg. Therefore, the Examiner respectfully is requested to withdraw this rejection and permit these claims to pass to allowance.

IV. NEW CLAIMS

New claims 15-20 are added to provide more varied protection for the present invention. No new matter is added. Particularly, claims 15-20 are directed to the subject matter of the illustrative, non-limiting embodiments of the present invention described, for example, at page 15, lines 24-27; page 17, lines 17-25; and page 18, lines 8-20.

Claims 15-20 are patentable over the cited references at least by virtue of their dependency from claim 1, and therefore, the Examiner is respectfully requested to allow the same.

V. FORMAL MATTERS AND CONCLUSION

Applicant thanks the Examiner for acknowledging Applicant's claim for foreign priority and for considering the references listed in the IDS filed on July 7, 2003.

Figures 1 and 3 are amended herewith to correct a minor spelling error (particularly, at reference numeral 8, the designation"DIGIT LINE". The Examiner respectfully is requested to acknowledge and approve the corrected drawings attached herewith. Annotated sheets showing changes have been included for the Examiner's convenience.

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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